IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

PARKERVISION, INC., Plaintiff, **v.** **LG ELECTRONICS, INC.,** Defendant.	**Case No. 6:21-cv-00520-ADA** **JURY TRIAL DEMANDED**

JOINT CLAIM CONSTRUCTION STATEMENT

I. TERMS THAT THE PARTIES NEWLY BRIEFED IN THIS LITIGATION

Term No.	Term	ParkerVision's Proposed Construction	LGE's Proposed Construction
1	"storage module" ('706 patent, cls. 105, 114, 115, 164, 166, 168, 175, 179, 186, 190; '835 patent, cls. 1, 18; '725 patent, cls. 1, 6, 17-19)	**Energy storage element / storage element:** "an element of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal" **Energy storage module / storage module:** "a module of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal" **Energy storage device**: "a device of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal"	"a module that stores a non-negligible amount of energy from an input electromagnetic (EM) signal"
	"energy storage module" ('902 patent, cl. 1)		
	"storage element" ('444 patent, cls. 3, 4)		
	"storage device" ('835 patent, cl. 20)		
	"energy storage element" ('513 patent, cl. 19; '528 patent, cls. 1, 9; '736 patent, cls. 1, 11, 21, 26, 27)		
	"energy storage device" ('673 patent, cls. 13, 17, 18)		
2	"A cable modem for down-converting an electromagnetic signal having complex modulations, comprising" ('835 patent, cl. 1)	The entire preamble (including "cable modem") is limiting.	Only the portion of the preamble reciting "an electromagnetic signal having complex modulations" is limiting.

II. TERMS WITH BRIEFING IN PRIOR LITIGATIONS INCORPORATED BY REFERENCE

Term No.	Term	ParkerVision's Proposed Construction and Citation(s) to Incorporated By Reference Arguments from Prior Litigations	LGE's Proposed Construction and Citation(s) to Incorporated By Reference Arguments from Prior Litigations
3	"said input sample" ('706 patent, cls. 1, 6, 7) "said sample" ('706 patent, cl. 34)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 9-10, § V.B; Dkt. No. 36-13: PV 562 Rep. Br. at 12-13, § IV.C	"the sample of the image that has been down-converted" **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 7, § II.B; Dkt. No. 32-55: Intel 562 Rep. Br. at 7-8, § II.B
4	"under-sample" / "under-samples" / "under-sampling" ('706 patent, cls. 1, 6, 7, 28, 34; '444 patent, cl. 2)	"sampling at an aliasing rate" or "sampling at less than or equal to twice the frequency of the input signal" **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 27-28, § IV.G; Dkt. No. 36-5: PV 108 Resp. Br. at 2-4, § II; 20-23, § III.G; Dkt. No. 36-6: PV 108 Rep. Br. at 3, § III; 16-17, § V.G; Dkt. No. 36-16: PV 870/945 Resp. Br. at 33-34, § IV.N	"sampling at less than or equal to twice the frequency of the input signal" **Citation(s):** Dkt. No. 33: Intel 108 Op. Br. at 19-24, § IV.B; Dkt. No. 32-90: Intel 108 Resp. Br. at 2-5, § II; 18-22, § III.B; Dkt. No. 32-97: Intel 108 Rep. Br. at 1-3, § II; 6-9, § III.B; Dkt. No. 32-18: TCL/Hisense Op. Br. at 31, § II.N; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 15, § I.I
5	"harmonic" / "harmonics" ('706 patent, cls. 1, 6, 7, 28, 34; '518 patent, cl. 1)	**Harmonic**: "A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic waveform and including the fundamental frequency as the first harmonic"	**Harmonic**: "A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic wave"

		Harmonics: "A frequency or tone that, when compared to its fundamental or reference frequency or tone, is an integer multiple of it and including the fundamental frequency as the first harmonic" **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 12-17, § V.D; Dkt. No. 36-13: PV 562 Rep. Br. at 7-8, § III; 15-17, § IV.E Dkt. No. 36-16: PV 870/945 Resp. Br. at 34-36, § IV.O; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 14, § VIII	**Harmonics**: "Sinusoidal components of a periodic wave each of which have a frequency that is an integer multiple of the fundamental frequency of the periodic wave" **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 10-12, § II.D; Dkt. No. 32-55: Intel 562 Rep. Br. at 9-12, § II.D; Dkt. No. 32-18: TCL/Hisense Op. Br. at 31-32, § II.O; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 15, § I.J
6	"integral filter/frequency translator to filter and down-convert an input signal" ('706 patent, cl. 28)	*Plain and ordinary meaning* wherein the plain-and-ordinary meaning is "a circuit having a unified input filter and frequency translator." **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 30-33, § V.I; Dkt. No. 36-13: PV 562 Rep. Br. at 4-6, § II.B; 25-26, § IV.J Dkt. No. 36-16: PV 870/945 Resp. Br. at 36-37, §IV.P; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 14, § VII	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 32, § II.P; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.H
7	"modulated signal" ('706 patent, cl. 127) "modulated carrier signal" ('513 patent, cl. 19;	"an electromagnetic signal at a transmission frequency having at least one characteristic that has been modulated by a baseband signal"	*Plain and ordinary meaning* **Citation(s):**

	’528 patent, cls. 1, 5, 14; ’736 patent, cls. 1, 11, 15; ’673 patent, cls. 1, 2, 7, 13, 19)	**Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 17-19, § IV.B; Dkt. No. 36-5: PV 108 Resp. Br. at 10-11, § III.B; Dkt. No. 36-6: PV 108 Rep. Br. at 4-5, § IV; 7-8, § V.B Dkt. No. 36-8: PV 562 Op. Br. at 35-36, § V.L; Dkt. No. 36-13: PV 562 Rep. Br. at 26-27, § IV.K; Dkt. No. 36-16: PV 870/945 Resp. Br. at 37-38, § IV.Q; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 14, § VII	Dkt. No. 32-18: TCL/Hisense Op. Br. at 32-33, § II.Q; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.H
8	“switch” (’706 patent, cls. 105, 107, 109, 111, 114, 115, 164, 165, 166, 168, 175, 176, 179, 186, 187, 190; ’518 patent, cl. 50; ’444 patent, cl. 3; ’835 patent, cls. 18, 19, 20; ’513 patent, cl. 19; ’528 patent, cls. 1, 5, 8, 17; ’736 patent, cls. 1, 11, 15, 21, 26, 27; ’673 patent, cls. 1, 6, 7, 13, 17, 18)	*Plain and ordinary meaning* wherein the plain-and-ordinary meaning is “an electronic device for opening and closing a circuit as dictated by an independent control input” **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 19-21, § IV.C; Dkt. No. 36-5: PV 108 Resp. Br. at 12-15, § III.C; Dkt. No. 36-6: PV 108 Rep. Br. at 4-5, § IV; 8-9, § V.C; Dkt. No. 36-16: PV 870/945 Resp. Br. at 43-44, § IV.V; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 14, § VII	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 33: Intel 108 Op. Br. at 41-43, § IV.I; Dkt. No. 32-90: Intel 108 Resp. Br. at 40-42, § III.I; Dkt. No. 32-97: Intel 108 Rep. Br. at 15, § III.I; Dkt. No. 32-18: TCL/Hisense Op. Br. at 36, § II.V; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.H
	“switch module” (’902 patent, cl. 1)		
	“switching device”		

	('725 patent, cl. 1)		
9	"universal frequency down-converter (UFD)" ('518 patent, cl. 50)	"circuitry that generates a down converted output signal from an input signal from a wide range of electromagnetic frequencies" **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 31-32, § IV.J; Dkt. No. 36-5: PV 108 Resp. Br. at 28-29, § III.H.4; Dkt. No. 36-6: PV 108 Rep. Br. at 4-5, § IV; Dkt. No. 36-16: PV 870/945 Resp. Br. at 38-40, § IV.R; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 14, § VII	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 33-34, § II.R; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.H
10	"a down-converted signal being generated from said sampled energy" ('902 patent, cl. 1)	"a lower frequency signal formed from sampled energy transferred from the electromagnetic signal when the switch module is closed and from sampled energy discharged from the storage module when the switch module is open" **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 23-26, § IV.E; Dkt. No. 36-5: PV 108 Resp. Br. at 15-19, § III.E; Dkt. No. 36-6: PV 108 Rep. Br. at 10-13, § V.E; Dkt. No. 36-16: PV 870/945 Resp. Br. at 44-45, § IV.W; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 15-17, § XI	"a down-converted signal being created from sampled energy stored in the energy storage module" **Citation(s):** Dkt. No. 33: Intel 108 Op. Br. at 43-45 , § IV.J; Dkt. No. 32-90: Intel 108 Resp. Br. at 42-44, § III.J; Dkt. No. 32-97: Intel 108 Rep. Br. at 16-17, § III.J; Dkt. No. 32-18: TCL/Hisense Op. Br. at 37-39, § II.W; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 15-17, § I.M

11	"frequency down-conversion module" ('444 patent, cls. 2, 3; '673 patent, cl. 1)	Not subject to § 112, ¶ 6 *Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 29-31, § IV.I; Dkt. No. 36-5: PV 108 Resp. Br. at 27-28, § III.H.3; Dkt. No. 36-6: PV 108 Rep. Br. at 17-20, § V.H; Dkt. No. 36-16: PV 870/945 Resp. Br. at 32-33, § IV.M; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § VI	Subject to § 112, ¶ 6 **Function**: "to down-convert the input signal ... according to a [] control signal and output[] a [] down-converted signal." **Structure**: an "aliasing module 2000" comprising at least one switch and one capacitor (Figures 20A and 20A-1). **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 30, § II.M; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.F, G
12	"system for frequency down-converting" ('513 patent, cl. 19; '528 patent, cl. 1; '736 patent, cl. 1) "apparatus for down-converting" ('673 patent, cl. 13)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 28-29, § IV.H; Dkt. No. 36-5: PV 108 Resp. Br. at 4-5, § II.C; 23, 25-27, § III.H, H.2; Dkt. No. 36-6: PV 108 Rep. Br. at 17-20, § V.H	"A system that down-converts a modulated carrier signal at an aliasing rate (i.e., by sampling at less than or equal to twice the frequency of the modulated carrier signal)" **Citation(s):** Dkt. No. 33: Intel 108 Op. Br. at 9-18, § IV.A; Dkt. No. 32-90: Intel 108 Resp. Br. at 2-5, § II; 5-18, § III.A; Dkt. No. 32-97: Intel 108 Rep. Br. at 3-6, § III.A
13	[wherein said storage elements comprises] "a capacitor that reduces a DC offset voltage in said first down-converted signal	*Plain and ordinary meaning* wherein the "a capacitor" in each of the storage elements reduces a DC offset voltage in the corresponding down-converted signal **Citation(s):**	[wherein said storage elements comprises] "a capacitor that reduces a DC offset voltage in both said first down-converted signal and said second down-converted signal" **Citation(s):**

	and said second down-converted signal" ('444 patent, cl. 4)	Dkt. No. 36-1: PV 108 Op. Br. at 34-37, § IV.M; Dkt. No. 36-5: PV 108 Resp. Br. at 30-31, § III.I; Dkt. No. 36-6: PV 108 Rep. Br. at 20-21, § V.I; Dkt. No. 36-16: PV 870/945 Resp. Br. at 40-41, § IV.S; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 14-15, § IX	Dkt. No. 33: Intel 108 Op. Br. at 29-32, § IV.D; Dkt. No. 32-90: Intel 108 Resp. Br. at 27-30, § III.D; Dkt. No. 32-97: Intel 108 Rep. Br. at 10-11, § III.D; Dkt. No. 32-18: TCL/Hisense Op. Br. at 34, § II.S; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 15, § I.K
14	"DC offset voltage" ('444 patent, cl. 4)	*Plain and ordinary meaning* wherein the plain-and-ordinary meaning is "the difference between the DC voltage of a signal and a reference voltage, *e.g.*, ground" **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 37-38, § IV.N; Dkt. No. 36-5: PV 108 Resp. Br. at 31-32, § III.J; Dkt. No. 36-6: PV 108 Rep. Br. at 21, § V.J Dkt. No. 36-16: PV 870/945 Resp. Br. at 41-42, § IV.T; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 14, § VII	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 34-35, § II.T; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.H
15	"sampling aperture" ('513 patent, cl. 19; '528 patent, cl. 1; '736 patent, cls. 1, 11; '673 patent, cls. 13, 17, 19)	"a period of time during which the switch is in its closed (*i.e.*, on) state" **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 21-23, § IV.D; Dkt. No. 36-5: PV 108 Resp. Br. at 15, § III.D;	"a period of time during which the switch is in its closed (*i.e.*, on) state as part of the process of reducing a continuous-time signal to a discrete-time signal" **Citation(s):** Dkt. No. 33: Intel 108 Op. Br. at 39-41 , § IV.H;

		Dkt. No. 36-6: PV 108 Rep. Br. at 9, § V.D; Dkt. No. 36-16: PV 870/945 Resp. Br. at 42-43, § IV.U; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 15, § X	Dkt. No. 32-90: Intel 108 Resp. Br. at 38-40, § III.H; Dkt. No. 32-97: Intel 108 Rep. Br. at 14, § III.H; Dkt. No. 32-18: TCL/Hisense Op. Br. at 35-36, § II.U; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 15, § I.L
16	"means for under-sampling an input signal to produce an input sample of a down-converted image of said input signal" ('706 patent, cl. 6)	**Function**: "under-sampling an input signal to produce an input sample of a down-converted image of the input signal and under-sampling the input signal according to a control signal" **Structure**: "switch 2650 in Fig. 26; switch 5308 in Figs. 53A/53A-1; and equivalents thereof" **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 20-23, § V.F; Dkt. No. 36-13: PV 562 Rep. Br. at 6-7, § II.C; 19-21, § IV.G; Dkt. No. 36-16: PV 870/945 Resp. Br. at 24-26, § IV.H; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § VI	Subject to § 112, ¶ 6 **Function**: "under-sampling an input signal to produce an input sample of a down-converted image of said input signal and under-sampling the input signal according to a control signal" **Structure**: "the switch 2650 and the capacitor 2652 in Fig. 26; the switch 5308 and capacitor 5310 in Figs. 53A/53A-1, and equivalents thereof" **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 13-17, § II.F; Dkt. No. 32-55: Intel 562 Rep. Br. at 14-17, § II.F; Dkt. No. 32-18: TCL/Hisense Op. Br. at 22-24, § II.H; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.G
17	"first delaying means for delaying said input sample"	**Function**: "delaying the input sample of a down-converted image of said input signal"	Subject to § 112, ¶ 6 **Function**: "delaying said input sample"

	('706 patent, cl. 6)	**Structure**: "capacitor 2656 in Fig. 26 or capacitor 5310 in Figs. 53A/53A1; and equivalents thereof" **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 23-25, § V.G; Dkt. No. 36-13: PV 562 Rep. Br. at 4-6, § II.B; 21-24, § IV.H; Dkt. No. 36-16: PV 870/945 Resp. Br. at 26-29, § IV.I; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § VI	**Structure**: "switch 2654 and capacitor 2656 shown in Fig. 26" **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 17-19, § II.G; Dkt. No. 32-55: Intel 562 Rep. Br. at 17-20, § II.G; Dkt. No. 32-18: TCL/Hisense Op. Br. at 24-26, § II.I; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.G
18	"second delaying means for delaying instances of an output signal" ('706 patent, cl. 6)	**Function**: delaying instances of an output signal **Structure**: delay modules 1722A, 1722B, 1722C, etc. in FIG. 17; delay modules 1912, 1914 in Fig. 19; delay modules 2316, 2318 in Fig. 23; first delay module 2628, second delay module 2630 in Fig. 26; delay module 3204 shown in Fig. 32; sample and hold circuits 4501, 4503 shown in Fig. 45; analog delay line 3404 shown in Fig. 34 having a combination of capacitors, inductors, and/or resistors; and equivalents thereof **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 25-30, § V.H; Dkt. No. 36-13: PV 562 Rep. Br. at 6-7, § II.C; 24-25, § IV.I	Subject to § 112, ¶ 6 **Function**: delaying instances of an output signal **Structure**: structure including "first delay module 2628," "second delay module 2630" shown in Fig 26 and described at 32:27-55, "delay module 3204" shown in Fig. 32 and described at 35:1-18; the sample and hold circuits 4501 and 4503 in Fig. 45 and described at 32:44-64; or an analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; and equivalents thereof. **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 19-22, § II.H;

			Dkt. No. 32-55: Intel 562 Rep. Br. at 20-22, § II.H
19	"filter tuning means for tuning one or more filter parameters" ('706 patent, cl. 134)	**Function**: tuning one or more filter parameters **Structure**: scaling modules 1716A, 1716B, 1716C, 1724A, 1724B, 1724C in Fig. 17; control signal generator 1790 in Fig. 17; input scaling module 1909 in Fig. 19; scaling modules 1916, 1918 in Fig. 19; scaling modules 2312, 2320, 2322 in Fig. 23; scaling module 2632, 2634 in Fig. 26; scaling module 3502 including resistor attenuator 3504, 3602 in Figs. 35, 36; scaling module 3702 including amplifier/attenuator 3704 in Fig. 37; control signal generator 4202 in Fig. 42; and equivalents thereof **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 36-43, § V.M; Dkt. No. 36-13: PV 562 Rep. Br. at 27-29, § IV.L	Subject to § 112, ¶ 6 **Function**: tuning one or more filter parameters **Structure**: scaling modules including the resistor attenuator 3602 (shown in Fig. 36 and described at 35:44-55) or the amplifier/attenuator 3704 implemented using operational amplifiers, transistors, or FETS (shown in Fig. 37 and described at 35:60-67), each of the resistor attenuator 3602 and the amplifier/attenuator 3704 having tunable resistors, capacitors, or inductors (as described at 42:33-36); and equivalents thereof; OR the control signal generator 4202 (shown in Fig. 42 and described at 36:44-62 and 42:27-32) implemented with a tunable oscillator 4204 and an aperture optimizing module 4210 using tunable components (such as tunable resistors, capacitors, inductors, etc.) (described at 36:63-37:5 and 42:27-32) and equivalents thereof. **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 25-28, § II.K; Dkt. No. 32-55: Intel 562 Rep. Br. at 24-26, § II.K

20	"a frequency translator to produce a sample of a down-converted image of an input signal, and to delay said sample" ('706 patent, cl. 34)	Not subject to § 112, ¶ 6 *Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 33-34, § V.J; Dkt. No. 36-13: PV 562 Rep. Br. at 4-7, §II.B-C; 12, § IV.B; Dkt. No. 36-16: PV 870/945 Resp. Br. at 29, § IV.J; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § VI	Subject to § 112, ¶ 6 **Function**: "produce a sample of a down-converted image of an input signal according to a control signal, and delay said sample" **Structure**: "the down-convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:20-41, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof" **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 3-7, § II.A; Dkt. No. 32-55: Intel 562 Rep. Br. at 2-7 , § II.A; Dkt. No. 32-18: TCL/Hisense Op. Br. at 26-27, § II.J; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.F, G
21	"a down-convert and delay module to under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample" ('706 patent, cls. 1, 7)	Not subject to § 112, ¶ 6 *Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 7-9, § V.A; Dkt. No. 36-13: PV 562 Rep. Br. at 1-7, § II.A-C; 8-10, § IV.A; Dkt. No. 36-16: PV 870/945 Resp. Br. at 19-20, § IV.E; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § VI	Subject to § 112, ¶ 6. **Function**: "under-sample an input signal according to a control signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample" **Structure**: "the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:20-41, that includes the

			switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof" **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 3-7, § II.A; Dkt. No. 32-55: Intel 562 Rep. Br. at 2-7 , § II.A; Dkt. No. 32-18: TCL/Hisense Op. Br. at 18-20, § II.E; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.F
22	"at least one delay module to delay instances of an output signal" ('706 patent, cls. 1, 7)	Not subject to § 112, ¶ 6 *Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 10-11, § V.C; Dkt. No. 36-13: PV 562 Rep. Br. at 1-3, §II.A; 6-7, §II.C; 13-15, § IV.D; Dkt. No. 36-16: PV 870/945 Resp. Br. at 20-21, § IV.F;	Subject to § 112, ¶ 6 **Function**: "delay instances of an output signal / further delay one or more of said delayed and down-converted input samples" **Structure**: "structure including "first delay module 2628," "second delay module 2630" shown in Fig 26, "delay module 3204" shown in Fig. 32 and described at 35:1-18; the sample and hold circuit 4501 and 4503 in Fig. 45 and described at 32:44-33:19; or an

	"at least one delay module to delay an output signal" ('706 patent, cl. 34)	Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § VI	analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; or equivalents thereof" **Citation(s):** Dkt. No. 32-45: Intel 562 Resp. Br. at 7-9, § II.C; Dkt. No. 32-55: Intel 562 Rep. Br. at 8-9 , § II.C; Dkt. No. 32-18: TCL/Hisense Op. Br. at 20-21, § II.F; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 14, § I.F, G
23	"said control signal comprises a train of pulses having pulse widths that are established to improve energy transfer from said input signal to said down-converted image" ('706 patent, cl. 2)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-8: PV 562 Op. Br. at 17-20, § V.E; Dkt. No. 36-13: PV 562 Rep. Br. at 18-19, § IV.F; Dkt. No. 36-16: PV 870/945 Resp. Br. at 21-23, § IV.G; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § V	Indefinite **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 21-22, § II.G; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 13-14, § I.E
24	"said energy transfer signal generator establishes apertures of said pulses to increase the time that said switch is closed for a purpose of reducing an impedance of said switch" ('706 patent, cl. 107)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-16: PV 870/945 Resp. Br. at 31-32, § IV.L; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § V	Indefinite **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 29-30, § II.L; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 13-14, § I.E

	"said energy transfer signal generator establishing apertures of said pulses to increase the time that said switch is closed to reduce an impedance of said switch, and to increase energy transferred from said input signal" ('706 patent, cls. 165, 176, 187)		
25	"between six and fifty percent of the energy transferred from the RF information signal to the storage module is discharged from the storage module" ('725 patent, cl. 17)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 38-39, § IV.O; Dkt. No. 36-5: PV 108 Resp. Br. at 32-35, 37-39, § III.K, K.1, K.4; Dkt. No. 36-6: PV 108 Rep. Br. at 21, § V.K	Indefinite **Citation(s):** Dkt. No. 33: Intel 108 Op. Br. at 45-48, § IV.K; Dkt. No. 32-90: Intel 108 Resp. Br. at 44-45, § III.K; Dkt. No. 32-97: Intel 108 Rep. Br. at 17-20, § III.K
	"between six and twenty-five percent of the energy transferred from the RF information signal to the storage module when is discharged from the storage module." ('725 patent, cl. 18)		
	"between ten and twenty percent of the energy transferred from the RF information signal to the storage module discharged from the storage module"		

	('725 patent, cl. 19) "the energy discharged during any given discharge cycle is not completely discharged" ('528 patent, cl. 9; '736 patent, cls. 1, 11)		
26	"low impedance load" ('736 patent, cls. 26, 27; '673 patent, cls. 5, 17) "said enemy[sic] discharged from said capacitor provides sufficient power to drive the low impedance load." ('673 patent, cl. 5)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-16: PV 870/945 Resp. Br. at 2-8, § IV.A-B; Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 1-6, § I-II	Indefinite **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 2-9, § II.A, B; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 1-5, § I.A, B
27	"wherein said energy transfer signal generator in widening said apertures of said pulses by a non-negligible amount that tends away from zero time in duration to extend the time that said switch is closed for the purpose of increasing energy transferred from said input signal does so at the expense of reproducing said input signal, such that said increased energy transferred from said input signal when said switch is	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-16: PV 870/945 Resp. Br. at 30, § IV.K Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 13, § V	Indefinite **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 27-28, § II.K; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 13-14, § I.E

	closed in response to said energy transfer signal prevents substantial voltage reproduction of said input signal" ('706 patent, cl. 111)		
28	"substantially the same size" ('902 patent, cl. 5)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 38-39, § IV.O; Dkt. No. 36-5: PV 108 Resp. Br. at 36-37, § III.K.3 Dkt. No. 36-6: PV 108 Rep. Br. at 21, § V.K	Indefinite **Citation(s):** Dkt. No. 33: Intel 108 Op. Br. at 45, 49-50, § IV.K; Dkt. No. 32-90: Intel 108 Resp. Br. at 44-45, § III.K; Dkt. No. 32-97: Intel 108 Rep. Br. at 21, § III.K
29	"separate integration module" ('528 patent, cl. 17)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-1: PV 108 Op. Br. at 38-39, § IV.O; Dkt. No. 36-5: PV 108 Resp. Br. at 35, § III.K.2 Dkt. No. 36-6: PV 108 Rep. Br. at 21, § V.K	Indefinite **Citation(s):** Dkt. No. 33: Intel 108 Op. Br. at 45, 48-49, § IV.K; Dkt. No. 32-90: Intel 108 Resp. Br. at 44-45, § III.K; Dkt. No. 32-97: Intel 108 Rep. Br. at 20-21, § III.K
30	"voltage of the input modulated carrier signal is not reproduced or approximated at the capacitor during the apertures or outside of the apertures" ('673 patent, cl. 2)	*Plain and ordinary meaning* **Citation(s):** Dkt. No. 36-16: PV 870/945 Resp. Br. at 16-19, § IV.D Dkt. No. 36-22: PV 870/945 Sur-Rep. Br. at 10-13, § IV	Indefinite **Citation(s):** Dkt. No. 32-18: TCL/Hisense Op. Br. at 16-18, § II.D; Dkt. No. 32-42: TCL/Hisense Rep. Br. at 12-13, § I.D

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that, on April 20, 2022, all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document.

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